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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/631,198	08/03/2000	Michael A. Lamson	TI-28674	9326

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EXAMINER

NGUYEN, DILINH P

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/631,198

Applicant(s)

LAMSON ET AL.

Examiner

DiLinh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 and 30-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-22 is/are allowed.
- 6) ☒ Claim(s) 30-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) ☐ Other: _____

DETAILED ACTION

The final rejection in paper No. 6 has been withdrawn. However, in view of further search the new final rejection has been made.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 30-31 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Stearns et al. (U.S. Pat. 6160705).

Stearns et al. disclose a semiconductor device comprising:

a substrate 14 (cover fig.) having first and second opposing surfaces, the substrate comprising:

a signal lines 22, a plurality of first power lines, and a plurality of second power lines on the second surface (fig. 6, column 7, lines 20 et seq.); wherein one or more of the plurality of signal lines 22 is between a pair of the plurality of first power lines 50 and 56, and further wherein the signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines are between a pair of the second power lines 58;

an integrated circuit chip 28 is mounted on the substrate.

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- Regarding claim 31, Stearns et al. disclose the signal lines are of a first width, the first power lines are of a second width, and the second power lines are of a third width.
- Regarding claim 33, Stearns et al. disclose a ground plane 16 on first surface of the substrate (fig. 1, column 4, lines 47-51).

3. Claim 34 is rejected under 35 U.S.C. 102(e) as being anticipated by Nemoto et al. (U.S. 6407432).

Nemoto et al. disclose a semiconductor device (fig. 13a) comprising:

a substrate having first and second opposing surfaces, the substrate comprising:

a plurality of lines of at least three different widths on the second surface of the substrate, wherein the lines are arranged such that one or more lines in a first set of lines of a first width are between lines of the second width, and such that one or more lines in a second set of lines of the second width are between lines of the third width; and

an integrated circuit chip 1 mounted on the substrate.

4. Claims 30-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kalidas et al. (U.S. 6396136).

Kalidas et al. disclose a semiconductor device (figs. 4a-4c, column 5, lines 10 et seq.) comprising:

a substrate 420 having first and second opposing surfaces, the substrate comprising:

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a plurality of signal lines 401, a plurality of first power lines 402, and a plurality of second power lines 403 on the second surface, wherein one or more of the plurality of signal lines is between a pair of the plurality of first power lines, and further wherein the signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines are between a pair of the second power lines (figs. 4b-4c);

an integrated circuit chip 400 mounted on the substrate.

- Regarding claim 31, Kalidas et al. disclose the signal lines 401 are of a first width, the first power lines 402 are of a second width, and the second power lines 403 are of a third width.
- Regarding claim 32, Kalidas et al. disclose the third width is wider than the second width, and the second width is wider than the first width.
- Regarding claim 33, Kalidas et al. disclose a ground plane 404 (fig. 4a) on the first surface of the substrate.
- Regarding claim 34, Kalidas et al. disclose a substrate 420 having first and second opposing surfaces, the substrate comprising: a plurality of lines of at least three different widths on the second surface of the substrate, wherein the lines are arranged such that one or more lines in a first set 401 of lines of a first width are between lines of the second width 402, and such that one or more lines in a second set of lines of the second width are between lines of the third width 403; an integrated circuit chip 400 mounted on the substrate.
- Regarding claim 35, Kalidas et al. disclose the lines of the first width are signal lines 401, the lines of the second width are power lines 402 coupled to a first

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voltage potential (column 5, lines 55-63), and the liens of the third width are power lines coupled to a second voltage potential.

- Regarding claim 36, Kalidas et al. disclose a ground plane 404 on the first surface of the substrate.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 34 is rejected under 35 U.S.C. 102(b) as being anticipated by Link et al. (U.S. 5055704).

Link et al. disclose a semiconductor device (fig. 4) comprising:

a substrate having first and second opposing surfaces, the substrate comprising:

a plurality of lines of at least three different widths on the second surface of the substrate, wherein the lines are arranged such that one or more lines in a first set of lines of a first width are between lines of the second width, and such that one or more lines in a second set of lines of the second width are between lines of the third width; and

an integrated circuit chip 132 mounted on the substrate.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nemoto et al. in view of Cuvilliers et al. (U.S. Pat. 4617586).

Nemoto et al. disclose the claimed invention except for not specifically point out that a ground plane on the first surface of the substrate.

Cuvilliers et al. disclose a semiconductor device (cover fig.) comprising a ground plane 16 on the first surface of the substrate 14 (column 2, line 59 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Nemoto et al. to reduce the capacitance of the conductors for the semiconductor package, as shown by Cuvilliers et al.

Claims Allowed

Claims 1-22 are allowed (see the previous examiner's statement of reasons for allowance).

Conclusion

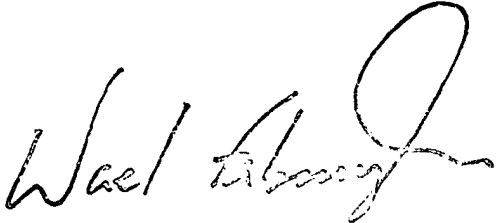
Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

– If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
August 19, 2003


SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2000